FORM PTO 1390
(REV 5-93) US DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. §371

ATTORNEY DOCKET NUMBER
2001-0565A

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)
09/891505
NEW

International Application No.	International Filing Date	Priority Date Claimed
PCT/JP00/06122	September 8, 2000	September 10, 1999

Title of Invention
SIGNAL PROCESSOR

Applicant(s) For DO/EO/US
Toru AOKI

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. §371.

2. [] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. §371.

3. [X] This express request to begin national examination procedures (35 U.S.C. §371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. §371(b) and PCT Articles 22 and 39(1).

4. [] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. [X] A copy of the International Application as filed (35 U.S.C. §371(c)(2))
   a. [] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [X] has been transmitted by the International Bureau. **ATTACHMENT A**
   c. [] is not required, as the application was filed in the United States Receiving Office (RO/US)

6. [X] A translation of the International Application into English (35 U.S.C. §371(c)(2)). **ATTACHMENT B**

7. [] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3)).
   a. [] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [] have been transmitted by the International Bureau.
   c. [] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [] have not been made and will not be made.

8. [] A translation of the amendments to the claims under PCT Article 19.

9. [X] An oath or declaration of the inventor(s) (35 U.S.C. §371(c)(4)). **ATTACHMENT C**

10. [] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. §371(c)(5)).

Items 11. to 14. below concern other document(s) or information included:

11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98. **ATTACHMENT D**

12. [] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. [X] A FIRST preliminary amendment. **ATTACHMENT E**

    [] A SECOND or SUBSEQUENT preliminary amendment.

14. [X] Other items or information: Notification Concerning Submission or Transmittal of Priority Document - **ATTACHMENT F**

JC03 Rec'd PCT/PTC 10 MAY 2001

U.S. APPLICATION NO. (if known, see 37 CFR 1.5) NEW 09/831505	INTERNATIONAL APPLICATION NO. PCT/JP00/06122	ATTORNEY'S DOCKET NO. 2001-0565A

15. [X] The following fees are submitted	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):		
Neither international preliminary examination fee nor international search fee paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00		
International Search Report has been prepared by the EPO or JPO ..... $ 860.00		
International preliminary examination fee not paid ot USPTO but international search paid to USPTO ..... $ 710.00		
International preliminary examination fee paid to USPTO but claims did not satisfy provisions of PCT Article 33(1)-(4) ..... $ 690.00		
International preliminary examination fee paid ot USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) ..... $ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	4 -20 =		X $18.00	$	
Independent Claims	1 - 3 =		X $80.00	$	
Multiple dependent claim(s) (if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$860.00	
[] Small Entity Status is hereby asserted. Above fees are reduced by 1/2.				$	
SUBTOTAL =				$860.00	
Processing fee of $130.00 for furnishing the English translation later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40 per property +				$	
TOTAL FEES ENCLOSED =				$860.00	
				Amount to be refunded	$
				Amount to be charged	$

a. [X] A check in the amount of $860.00 to cover the above fees is enclosed. A duplicate copy of this form is enclosed.

b. [] Please charge my Deposit Account No. 23-0975 in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 23-0975.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

19. CORRESPONDENCE ADDRESS

000513

PATENT TRADEMARK OFFICE

By: _____

Nils E. Pedersen,
Registration No. 33,145

WENDEROTH, LIND & PONACK, L.L.P.
2033 "K" Street, N.W., Suite 800
Washington, D.C. 20006-1021
Phone:(202) 721-8200
Fax:(202) 721-8250

May 10, 2001

AUTHORIZED

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY DEFICIENCY IN THE FEES FOR THIS PAPER TO DEPOSIT ACCOUNT NO. 23-0975

[CHECK NO. 44413]

[2001_0565A]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of :

Toru AOKI : **Attn: BOX PCT**

Serial No. NEW : **Docket No. 2001-0565A**

Filed May 10, 2001 :

SIGNAL PROCESSOR
[Corresponding to PCT/JP00/06122
Filed September 8, 2000]

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents,
Washington, DC 20231

Sir:

Prior to examination of the above-referenced U.S. patent application please amend the application as follows:

IN THE TITLE

Please change the title of the invention to:

SIGNAL PROCESSOR FOR CORRECTING AND DETECTING ERRORS.

IN THE ABSTRACT

Please replace the original abstract with the enclosed substitute abstract.

REMARKS

The present Preliminary Amendment is submitted to make minor editorial changes.

Attached hereto is a marked-up version of the changes made to the title and abstract by the current Preliminary Amendment. The attached page is captioned "**Version With Markings to Show Changes Made**".

Respectfully submitted,

Toru AOKI

By [signature]
Nils E. Pedersen
Registration No. 33,145
Attorney for Applicant

NEP/krl
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
May 10, 2001

THE COMMISSIONER IS AUTHORIZED TO CHARGE ANY DEFICIENCY IN THE FEES FOR THIS PAPER TO DEPOSIT ACCOUNT NO. 23-0975

DESCRIPTION

Version with Markings to Show Changes Made

SIGNAL PROCESSOR FOR CORRECTING AND DETECTING ERRORS

TECHNICAL FIELD

The present invention relates to a signal processor for detecting and correcting errors in data read from a recording medium.

BACKGROUND ART

In recent years, high quality and speedup are demanded of a DVD-ROM, which has become widespread as a digital memory, to increase the reliability of data read from a DVD disk. With the demand, a signal processor for correcting errors in the disk is required to have rapid processing means, and it is aimed at realization of high-speed data processing.

A conventional CD-ROM signal processor performs error correction by a predetermined number of times. Further, the CD-ROM signal processor writes inputted data in a buffer memory and, simultaneously, detects errors in the data by using CRC (Cyclic Redundancy Check). Based on the result of CRC, when the data is decided as "error-free data", the signal processor reduces the predetermined number of error corrections.

In the case of DVD-ROM data, however, since inputted data

ABSTRACT

In a signal processor according to the present invention, shown in figure 1, error correction is performed on data w h has been subjected to predetermined signal processing, fo ch predetermined block unit, by an error correction bloc 52, in parallel with the operation of sequentially stori the data in a cache memory 16. Then, error detection is per ed on the data for each predetermined block unit by a descrambling/error detection block 153, and the data is stored in a buffer memory 14. Based on the results of the error detection and the error correction, when there exists some error in the data, the data with the error, which is stored in the buffer memory 14, is read out to be subjected to error correction again. When there is no error, the data corresponding to one block and stored in the buffer memory 14 is transmitted to a host computer 13 without performing error correction again.

In the signal processor so constructed, the number of memory accesses can be reduced by reducing the number of error corrections, resulting in higher-speed data processing.

DESCRIPTION

SIGNAL PROCESSOR

TECHNICAL FIELD

The present invention relates to a signal processor for detecting and correcting errors in data read from a recording medium.

BACKGROUND ART

In recent years, high quality and speedup are demanded of a DVD-ROM, which has become widespread as a digital memory, to increase the reliability of data read from a DVD disk. With the demand, a signal processor for correcting errors in the disk is required to have rapid processing means, and it is aimed at realization of high-speed data processing.

A conventional CD-ROM signal processor performs error correction by a predetermined number of times. Further, the CD-ROM signal processor writes inputted data in a buffer memory and, simultaneously, detects errors in the data by using CRC (Cyclic Redundancy Check). Based on the result of CRC, when the data is decided as "error-free data", the signal processor reduces the predetermined number of error corrections.

In the case of DVD-ROM data, however, since inputted data

is not previously subjected to error correction in contrast to the CD-ROM data, the error rate is higher in the DVD-ROM data than in the CD-ROM data. Therefore, when the DVD-ROM data is subjected to CRC, the result of CRC is, in most cases, that there are errors in the DVD-ROM data.

Figure 6 is a block diagram illustrating the structure of a conventional DVD-ROM signal processor.

In figure 6, a DVD-ROM signal processor 65 receives DVD-ROM digital signal data (hereinafter referred to as "data") which is read by an optical pickup 61, and outputs the data after error correction to a host computer 63. The DVD-ROM signal processor 65 is under control of a control microcomputer 62, and is connected with a buffer memory 64 which stores data.

To be specific, the DVD-ROM signal processor 65 is provided with an FMT block 651 for capturing the DVD-ROM data outputted from the optical pickup 61, and storing it in the buffer memory 64; an error correction block 652 for correcting errors in the data stored in the buffer memory 64; a descrambling block 653 for descrambling the scrambled data; an error detection block 654 for detecting errors in the data after error correction, which data is stored in the buffer memory 64; a host interface block 655 for transmitting error-free data to the host computer, based on the result of the error detection by the error detection block 654; and a memory

interface block 656 for controlling the processing between the DVD-ROM signal processor 65 and the buffer memory 64.

The operation of the conventional DVD-ROM signal processor so constructed will be described with reference to figures 4 and 6.

Figure 4 is a diagram illustrating the data format constituting one ECC block.

As shown in figure 4, the logical format of the DVD-ROM data outputted from the optical pickup 61 is constituted with 182×208 bytes as one ECC (Error Correcting Code) block.

First of all, the data read by the optical pickup 61 forms one component unit with 182 bytes as a C1 code word. The C1 code word is composed of 172 bytes of user data and 10 bytes of C1 parity. One ECC block is composed of plural C1 code words and plural C2 code words, each C2 code word comprising 208 bytes obtained by collecting one byte from each C1 code word. Each C2 code word is composed of 192 bytes of user data and 16 bytes of C2 parity. The DVD-ROM data has been scrambled in advance.

In figure 6, the FMT block 651 converts the DVD-ROM serial data outputted from the optical pickup 61 into parallel data (serial to parallel conversion), subjects the converted data to demodulation and sync detection, and writes the parallel data in the buffer memory 64 through the memory interface block 656.

The error correction block 652 reads the DVD-ROM data written in the buffer memory 64, through the memory interface block 656, performs syndrome calculation on the C1 code words and the C2 code words shown in figure 4, and calculates the error position and the error pattern by using the result of the syndrome calculation. Based on the result of the syndrome calculation, the error correction block 652 terminates the error correction when the data has no error. However, when the data has some error, the error correction block 652 reads the error data stored in the buffer memory 64, through the memory interface block 656, performs error correction on the error data, and writes the corrected data over the address of the error data stored in the buffer memory 64, through the memory interface block 656.

The descrambling block 653 reads the DVD-ROM data which has been subjected to error correction and is stored in the buffer memory 64, through the memory interface block 656, descrambles the data according to a predetermined method, and writes the data in the buffer memory 64 through the memory interface block 656.

The error detection block 654 reads the DVD-ROM data which has been descrambled and is stored in the buffer memory 64, through the memory interface block 656, and detects errors in the read data by performing predetermined calculation.

The host interface block 655 transmits, to the host

computer 63, the DVD-ROM data which has been decided as "error-free data" in both of the error correction block 652 and the error detection block 654.

Each of the above-mentioned blocks is constructed so as to operate at a predetermined timing according to an instruction from the control microcomputer 62.

In the conventional DVD-ROM signal processor, however, when the DVD-ROM data is subjected to error correction, the following operations are performed on the buffer memory 64: writing of data from the FMT block 651, reading and writing of data from the error correction block 652, reading and writing of data from the descrambling block 653, reading of data from the error detection block 654, and reading of data from the host interface block 655. That is, since reading and writing of data are performed frequently through the buffer memory 64, the memory band width is pressed and, therefore, the signal processor cannot perform high-speed access and higher-speed data processing.

The present invention is made to solve the above-described problem, and it is an object of the present invention to provide a signal processor which can reduce the number of memory accesses by reducing the number of error corrections, thereby realizing higher-speed data processing.

DISCLOSURE OF THE INVENTION

A signal processor according to the present invention (Claim 1) is a signal processor for subjecting data read from a recording medium to predetermined digital signal processing, and subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block. This signal processor comprises: memory means for sequentially storing the data which has been subjected to the predetermined digital signal processing; error correction means for subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block; descrambling/error detection means for descrambling the data which has been subjected to the error correction, and detecting errors in the data after the descrambling; and control means for transmitting error-free data to a display unit when there is no error in the data which has been subjected to the error detection.

In the signal processor so constructed, the number of data error corrections can be reduced, whereby reduced power consumption of the device itself can be achieved. Further, since the number of memory accesses to the memory means for error correction can be reduced, the access right to the memory means can be assigned to another block, whereby high-speed processing of the signal processor is realized.

According to the present invention (Claim 2), in the

signal processor described in Claim 1, the error correction means comprises: a syndrome calculator for calculating syndrome of the data which has been subjected to the predetermined digital signal processing; an error position/pattern calculator for calculating the error position and the error pattern after the syndrome calculation; error correction result holding means for holding information as to whether the data detected by the error position/pattern calculator is error-correctable or not; data correction means for correcting errors in the data on the basis of the result of the syndrome calculation; and number-of-error-correction control means for controlling the number of error corrections.

In the signal processor so constructed, the time required for memory access to the memory means can be reduced by reducing the number of error corrections and, furthermore, speedup of data processing is achieved.

According to the present invention (Claim 3), in the signal processor described in Claim 1, the descrambling/error detection means comprises: descrambling means for descrambling the data which has been corrected by the error correction means; error detection means for detecting errors in the descrambled data; and error detection result holding means for holding the result of the error detection as to whether there is any error in the data which has been subjected to the error detection.

In the signal processor so constructed, based on the result of error detection, when there is no error, the data is transmitted to the host computer without performing error correction again, whereby the number of error corrections can be reduced. Accordingly, the power consumption of the device itself can be reduced.

According to the present invention (Claim 4), in the signal processor described in Claim 1, the data subjected to the predetermined digital signal processing is read from the memory means for each predetermined error correction block, followed by error detection and error correction; when there is some error, the error is corrected by the error correction means for each predetermined error correction block; when there is no error, the data is transmitted to the display means for each predetermined error correction block.

In the signal processor so constructed, the time required for memory access to the memory means can be reduced by terminating the second and more error corrections or reducing the number of error corrections for the data in each predetermined error correction block stored in the memory means, and further high-speed transmission of the data to the host computer is achieved.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating the structure of

a DVD-ROM signal processor according to a first embodiment of the present invention.

Figure 2 is a block diagram illustrating the internal structure of an error correction block according to a second embodiment of the present invention.

Figure 3 is a block diagram illustrating the internal structure of a descrambling/error detection block according to a third embodiment of the present invention.

Figure 4 is a diagram illustrating the data format constituting one ECC block.

Figure 5 is a timing chart of memory access in DVD-ROM signal processing according to a fourth embodiment.

Figure 6 is a block diagram illustrating the structure of the conventional DVD-ROM signal processor.

BEST MODE TO EXECUTE THE INVENTION

Embodiment 1.

Figure 1 is a block diagram illustrating the structure of a DVD-ROM signal processor according to a first embodiment of the present invention.

In figure 1, a DVD-ROM signal processor 15 receives DVD-ROM digital signal data (hereinafter referred to as "data") which is read by an optical pickup 11, and outputs the data after error correction to a host computer 13. The DVD-ROM signal processor 15 is controlled by a control microprocessor

12, and it connects a cache memory 16 for storing the data and to a buffer memory for storing the data stored in the cache memory 16.

To be specific, the DVD-ROM signal processor 15 is provided with an FMT block 151 for capturing the DVD-ROM data outputted from the optical pickup 11; an error correction block 152 for correcting errors in the data stored in the cache memory 16 and the buffer memory 14; a descrambling/error detection block 153 for descrambling the scrambled data, and detecting errors in the descrambled data; an error detection block 154 for detecting errors in the data which has been subjected to error correction and is stored in the buffer memory 14; a host interface block 155 for transmitting error-free data to the host computer 13, based on the result of error detection by the error detection block 154; a memory interface block B 156 for controlling the processing between the DVD-ROM signal processor 15 and the buffer memory 14; and a memory interface block A 157 for controlling the processing between the DVD-ROM signal processor 15 and the cache memory 16.

The operation of the signal processor so constructed will be described with reference to figures 1 and 4.

Figure 4 is a diagram illustrating the data format constituting one ECC block.

As shown in figure 4, the logical format of the DVD-ROM

data outputted from the optical pickup 11 is constituted with 182×208 bytes as one ECC block.

First of all, the data read by the optical pickup 11 forms one component unit with 182 bytes as a C1 code word. The C1 code word is composed of 172 bytes of user data and 10 bytes of C1 parity. One ECC block is composed of plural C1 code words and plural C2 code words, each C2 code word having 208 bytes obtained by collecting one byte from each C1 code word. Each C2 code word is composed of 192 bytes of user data and 16 bytes of C2 parity. The DVD-ROM data has been scrambled in advance.

Initially, with reference to figure 1, the DVD-ROM data outputted from the optical pickup 11 is converted from serial data to parallel data (serial to parallel conversion) by the FMT block 151. The parallel data are subjected to demodulation and sync detection, and one of the parallel data is written in the cache memory through the memory interface block A 157. At the same time, the other one of the parallel data is transmitted for each ECC block to the error correction block 152, wherein it is subjected to error correction. The data which has been subjected to error correction by the error correction block 152 is written in the cache memory 16 through the memory interface block A 157.

Next, the data after error correction is read from the cache memory 16 through the memory interface block A 157, and

the scrambled data is subjected to descrambling and error correction by the descrambling/error detection block 153, and the data is transmitted to the buffer memory 14 through the memory interface block B 156. At this time, when the descrambling/error detection block 153 detects some error in the data, error correction is carried out again by the error correction block 152.

The data which has been subjected to error correction by the error correction block 152 is inputted to the error detection block 154 through the buffer memory 14 and the memory interface block B 156, wherein error detection is carried out again. Based on the result of the error detection, only the data decided as "error-free data" is transmitted to the host computer 13 through the host interface block 155.

As described above, in the signal processor according to the first embodiment, the DVD-ROM data inputted to the signal processor is subjected to error detection and error correction for every ECC block. When the data has some error, the data is subjected to error correction for every ECC block. When the data has no error, the data is transmitted to the host computer 13 for every ECC block. Therefore, although in the conventional example error correction is carried out by a predetermined number of times, such wasteful correction work is avoided, and the number of error corrections is reduced. Accordingly, it is possible to reduce the power consumption of

the device itself. Further, since the number of memory accesses to the buffer memory 14 for error correction is reduced, the access right to the buffer memory 14 can be assigned to another block, whereby speedup of the signal processor is realized.

Embodiment 2.

Figure 2 is a block diagram illustrating the internal structure of an error correction block according to a second embodiment of the present invention.

With reference to figure 2, an error correction block 152 is provided with a syndrome calculator 1521 for performing syndrome calculation; a scrambling circuit 1522 for scrambling descrambled data; an error position/pattern calculation block 1523 for calculating the error position in data and the error pattern on the basis of the result from the syndrome calculator 1521, and detecting data having uncorrectable errors (hereinafter referred to as "error uncorrectable data"); an error correction result holding circuit 1524 for holding information as to whether there is error uncorrectable data or not, which is detected in the error position/pattern calculation block 1523; data correction circuit 1525 for correcting errors in the data according to the error position and the error pattern calculated from the syndrome by the error position/pattern calculation block 1523; and a number-of-error-correction control circuit 1526 for controlling the

number of error corrections.

The operation of the error correction block so constructed will be described with reference to figure 2.

Initially, in the above-described first embodiment, the DVD-ROM data transmitted to the error correction block 152 is inputted to the syndrome calculator 1521 for each ECC block, wherein the data is subjected to syndrome calculation. At this time, if there is some error at the point of time when 182 bytes of data equivalent to the C1 code word have been inputted, the result of the syndrome calculation is transmitted to the error position/pattern calculation block 1523, wherein the error position and the error pattern are calculated.

In the error position/pattern calculation block 1523, it is detected whether there is any uncorrectable error or not, and the information about the presence or absence of uncorrectable error is stored in the error correction result holding circuit 1524. The information about the presence or absence of uncorrectable error, which is stored in the error correction result holding circuit 1524, is output to the number-of-error-correction control circuit 1526.

On the other hand, the information about the error position and the error pattern calculated in the error position/pattern calculation block 1523 is transmitted to the data correction circuit 1525. The data correction circuit 1525

reads the data stored in the address indicated by the error position from the cache memory 16 through the memory interface block A 157, and performs error correction by using the error position and the error pattern calculated by the error position/pattern calculation block 1523. The data which has been subjected to error correction by the data correction circuit 1525 is written in the address indicating the error position which is stored in the cache memory, through the memory interface block A 157.

The data which has been subjected to the first error correction in this way is subjected to error detection in the descrambling/error detection block 153, and transmitted to the buffer memory 14 through the memory interface block B. At this time, when some error is detected in the descrambling/error detection block 153, error correction is again carried out in the error correction block 152. Hereinafter, this process will be described in more detail.

In figure 2, the number-of-error-correction control circuit 1526 decides whether there is any error in the data stored in the buffer memory 14, on the basis of the information from the error correction result holding circuit 1524 and the descrambling/error detection block 153 shown in figure 1. Based on the result of the detection, when there is no error, the number-of-error-correction control circuit 1526 outputs the status of "free from error" to the control

microcomputer 12. However, when there is some error in the data stored in the buffer memory 14, the number-of-error-correction control circuit 1526 outputs the status of "error" to the control microcomputer 12, and the syndrome calculator 1521 performs syndrome calculation again.

The syndrome calculator 1521 reads the data with error stored in the buffer memory 14, through the memory interface block B 156. The read data is initially subjected to scrambling by the scrambling circuit 1522, and then converted to the data that can be subjected to syndrome calculation. The converted data is inputted to the syndrome calculator 1521 for each ECC block, and subjected to syndrome calculation. If there is some error at the point of time when 182 bytes of data equivalent to the C1 code word or 208 bytes of data equivalent to the C2 code word have been inputted, the result of the syndrome calculation is transmitted to the error position/pattern calculation block 1523, wherein the error position and the error pattern are calculated.

Next, the information about the calculated error position and error pattern is transmitted to the data correction circuit 1525. The data correction circuit 1525 reads the data in the address indicating the error position from the buffer memory 14 through the memory interface block B156, and performs error correction by using the error position and the error pattern calculated by the error position/pattern

calculation block 1523. Then, the data which have been subjected to error correction in the data error correction circuit 1525 is written in the address indicating the error position of the data stored in the buffer memory 14, through the memory interface block B156.

As described above, in the signal processor according to the second embodiment, syndrome calculation is performed on the data of each ECC block unit, which is inputted to the error correction block 152, and then error correction is performed on the data of each ECC block unit according to the result of the calculation. Therefore, the number of error corrections can be reduced and, furthermore, the number of memory accesses to the memory means can be reduced. Accordingly, high-speed data processing can be achieved.

Embodiment 3.

Figure 3 is a block diagram illustrating the internal structure of a descrambling/error detection block according to a third embodiment of the present invention.

In figure 3, a descrambling/error detection block 153 is provided with a descrambling circuit 1531 for descrambling scrambled data; an error detection circuit 1532 for detecting errors in the descrambled data; and an error detection result holding circuit 1533 for holding the result of error detection (presence or absence of error) by the error detection circuit 1532.

The operation of the descrambling/error detection block so constructed will be described with reference to figure 3.

Initially, the data which has been subjected to error correction in the error correction block 152 is inputted to the descrambling circuit 1531 from the cache memory 16 through the memory interface block A 157, and the data is descrambled according to a predetermined method. The descrambled data is transmitted to the error detection circuit 1532, wherein errors in the data are detected by predetermined calculation. The data after the error detection is transmitted to the buffer memory 14 through the memory interface block B156. Further, information about the result of the error detection by the error detection circuit 1532 is latched in the error detection result holding circuit 1533, and then outputted to the number-of-error-correction control circuit 1526 (see figure 2) in the error correction block 152.

As described above, in the signal processor according to the third embodiment, the inputted data is descrambled and then subjected to error detection. Based on the result of the error detection, when there is no error, the data is transmitted to the host computer without performing data correction again. Therefore, the number of error corrections can be reduced, resulting in reduced power consumption of the signal processor.

Embodiment 4.

Figure 5 is a timing chart of memory access of a DVD-ROM signal processor according to a fourth embodiment of the present invention.

First of all, each of codes shown in figure 5 will be described.

N~N+3 denote block numbers of blocks when the data inputted to the DVD-ROM signal processor is subjected to error correction for each ECC block.

Process 1 denotes the process from when the data inputted to the DVD-ROM signal processor is inputted to the cache memory 16 and the error correction block 152 through the FMT block 151 to when the first error correction is carried out.

Process 2 denotes the process of performing the second and further error correction in the error correction block 152 when the data has some error in Process 1.

Process 3 denotes the process of transmitting error-free data to the host computer 13 through the host interface block 155 when the data has no error.

The operation of the DVD-ROM signal processor so constructed will be described with respect to tne timing of memory access, with reference to figure 5.

In figure 5, for example, the data corresponding to the Nth, (N+2)th, and (N+3)th blocks are constituted by the error-free or error correctable C1 code word while the data corresponding to the (N+1)th block includes the error

uncorrectable C1 code word.

Initially, with respect to the data in the Nth, (N+2)th, and (N+3)th blocks, these data having no errors at the point of time when Process 1 is ended are stored in the buffer memory 14. In this case, Process 1 is not followed by Process 2 but followed by Process 3 wherein the error-free data are transmitted for each ECC block to the host computer 13.

On the other hand, with respect to the data in the (N+1)th block, since this data has an error at the point of time when Process 1 is ended, Process 1 is followed by Process 2 wherein the error data is corrected. Those blocks containing the data which are finally decided as "error-free error" are transmitted to the host computer 13 in Process 3.

As described above, according to the signal processor of this fourth embodiment, the DVD-ROM data inputted to the signal processor is processed for every ECC block from when capture of the data is started to when the data is transmitted to the host computer 13. Therefore, in the case where Process 1 is performed on the data corresponding to one ECC block and then Process 3 is performed without performing Process 2 because there is no error, the access time inside the signal processor can be reduced by one ECC block. Accordingly, high-speed transmission of the data to the host computer 13 is realized.

APPLICABILITY IN INDISTORY

As described above, the signal processor according to the present invention can reduce the number of memory accesses by reducing the number of error corrections to process data at higher speed. Especially, it is suitable as a signal processor for which speedup is demanded, such as a DVD-ROM.

CLAIMS

1. A signal processor for subjecting data read from a recording medium to predetermined digital signal processing, and subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block, said signal processor comprising:

memory means for sequentially storing the data which has been subjected to the predetermined digital signal processing;

error correction means for subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block;

descrambling/error detection means for descrambling the data which has been subjected to the error correction, and detecting errors in the data after the descrambling; and

control means for transmitting error-free data to a display unit when there is no error in the data which has been subjected to the error detection.

2. A signal processor as described in Claim 1 wherein said error correction means comprises:

a syndrome calculator for calculating syndrome of the data which has been subjected to the predetermined digital signal

processing;

an error position/pattern calculator for calculating the error position and the error pattern after the syndrome calculation;

error correction result holding means for holding information as to whether the data detected by the error position/pattern calculator is error-correctable or not;

data correction means for correcting errors in the data on the basis of the result of the syndrome calculation; and

number-of-error-correction control means for controlling the number of error corrections.

3. A signal processor as described in Claim 1 wherein said descrambling/error detection means comprises:

descrambling means for descrambling the data which has been corrected by the error correction means;

error detection means for detecting errors in the descrambled data; and

error detection result holding means for holding the result of the error detection as to whether there is any error in the data which has been subjected to the error detection.

4. A signal processor as described in Claim 1 wherein:

the data subjected to the predetermined digital signal processing is read from the memory means for each

predetermined error correction block, followed by error detection and error correction;

when there is some error, the error is corrected by the error correction means for each predetermined error correction block;

when there is no error, the data is transmitted to the display means for each predetermined error correction block.

ABSTRACT

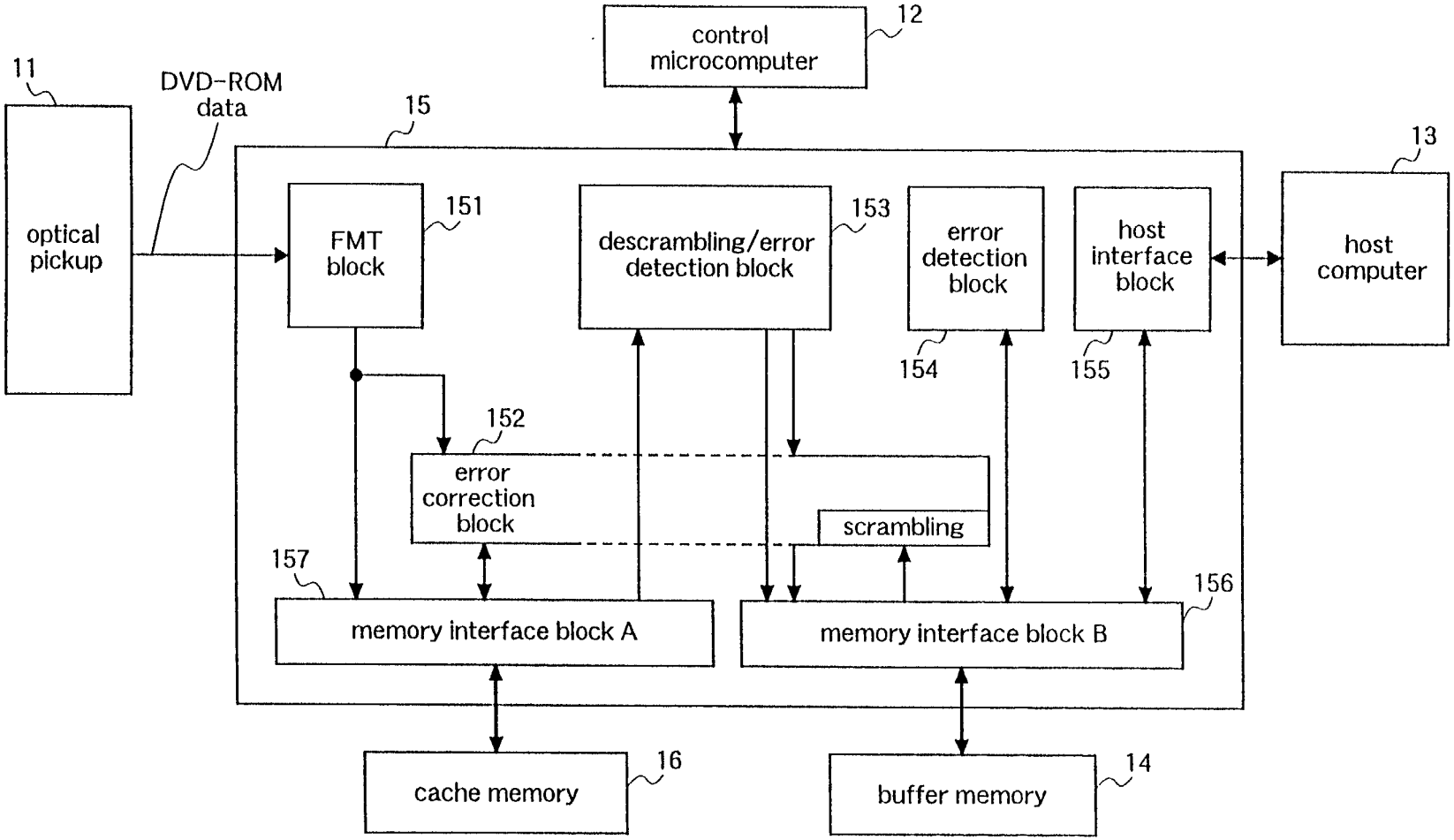
In a signal processor according to the present invention, as shown in figure 1, error correction is performed on data which has been subjected to predetermined signal processing, for each predetermined block unit, by an error correction block 152, in parallel with the operation of sequentially storing the data in a cache memory 16. Then, error detection is performed on the data for each predetermined block unit by a descrambling/error detection block 153, and the data is stored in a buffer memory 14. Based on the results of the error detection and the error correction, when there exists some error in the data, the data with the error, which is stored in the buffer memory 14, is read out to be subjected to error correction again. When there is no error, the data corresponding to one block and stored in the buffer memory 14 is transmitted to a host computer 13 without performing error correction again.

In the signal processor so constructed, the number of memory accesses can be reduced by reducing the number of error corrections, resulting in higher-speed data processing.

ABSTRACT

In a signal processor according to the present invention, as shown in figure 1, error correction is performed on data which has been subjected to predetermined signal processing, for each predetermined block unit, by an error correction block 152, in parallel with the operation of sequentially storing the data in a cache memory 16. Then, error detection is performed on the data for each predetermined block unit by a descrambling/error detection block 153, and the data is stored in a buffer memory 14. Based on the results of the error detection and the error correction, when there exists some error in the data, the data with the error, which is stored in th e buffer memory 14, is read out to be subjected to error correction again. When there is no error, the data corresponding to one block and stored in the buffer memory 14 is transmitted to a host computer 13 without performing error correction again.

Fig.1



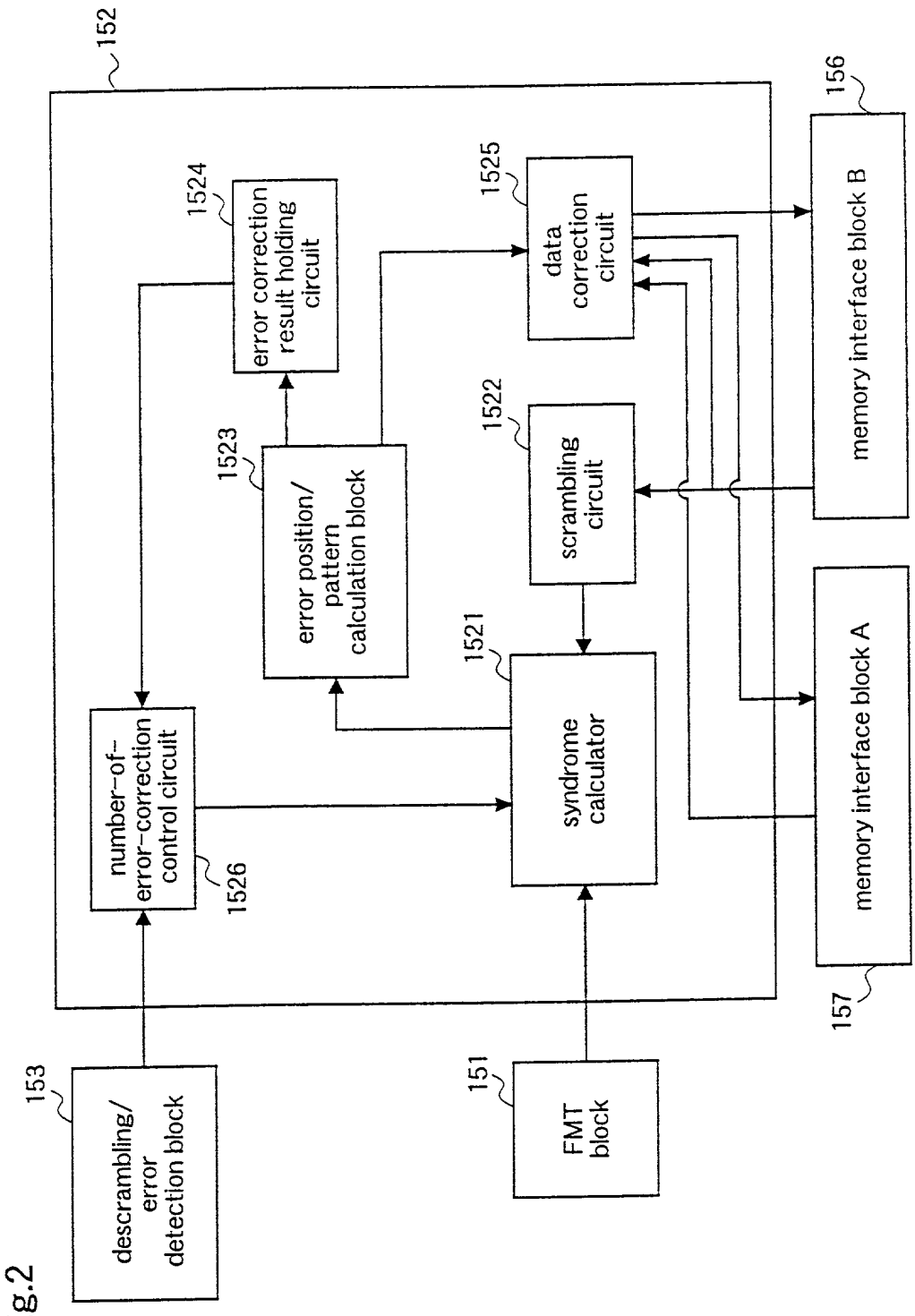


Fig.2

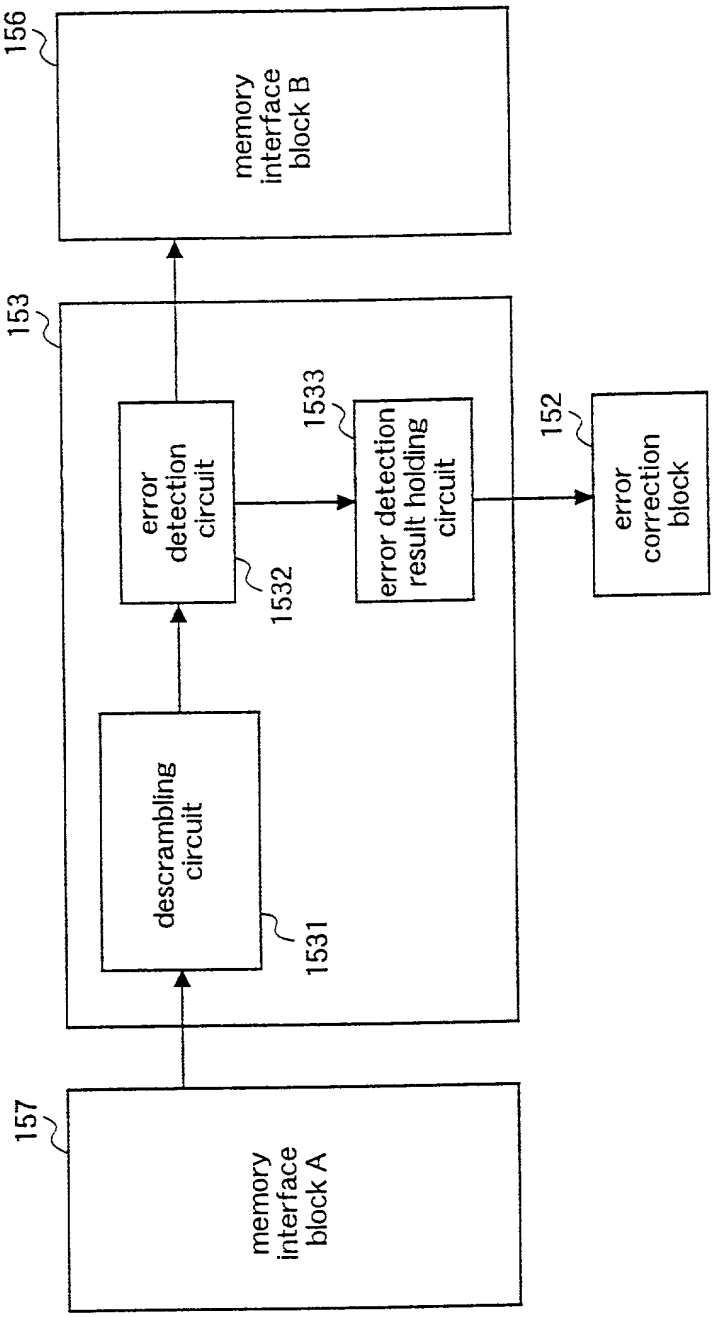

156
memory interface block B
153
error detection circuit
1533
error detection result holding circuit
152
error correction block
1532
descrambling circuit
1531
157
memory interface block A

Fig.3

Fig.4

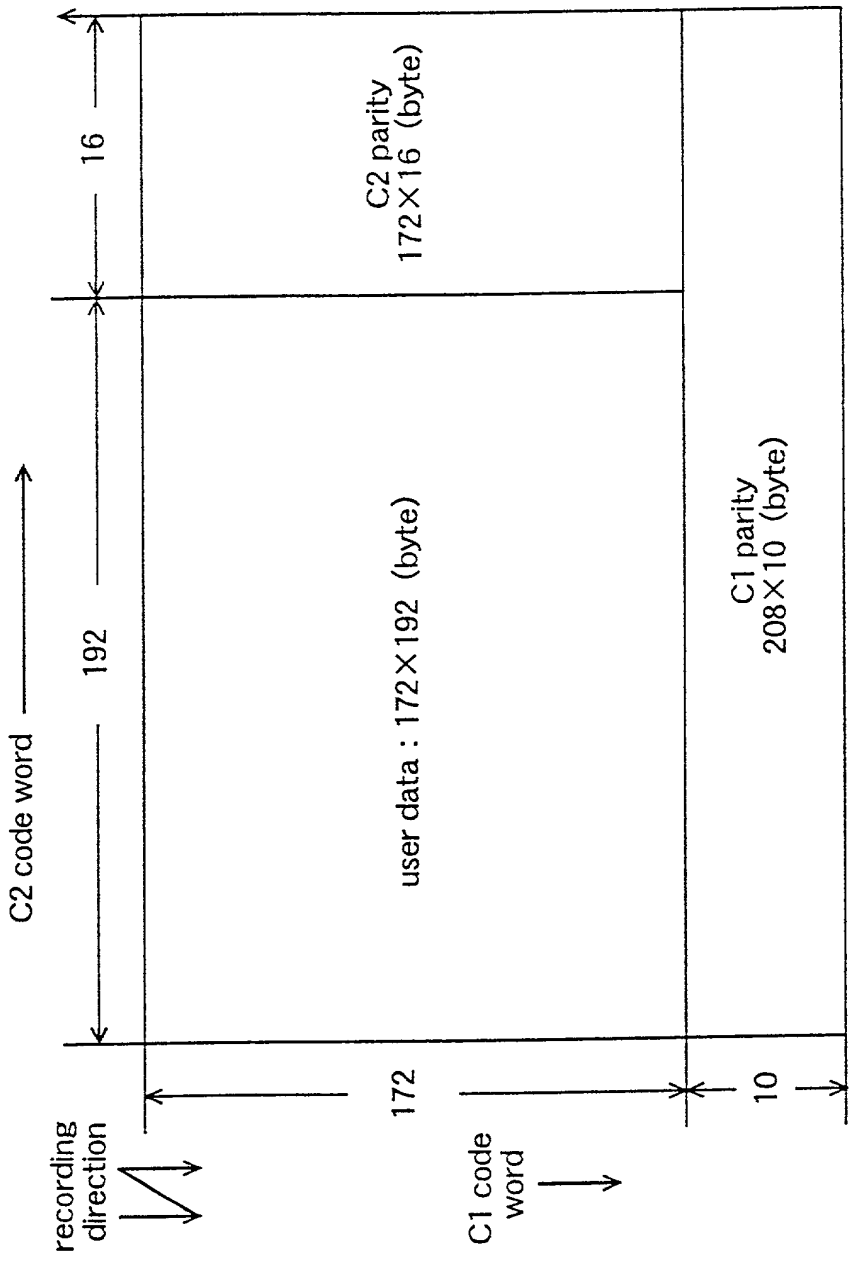
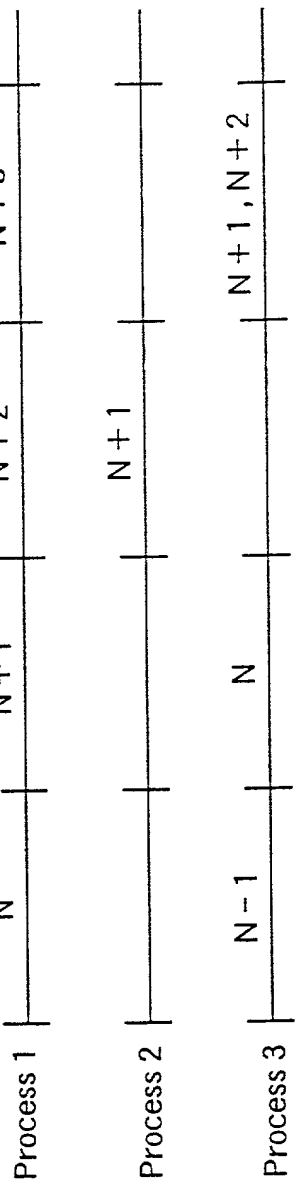


Fig.5



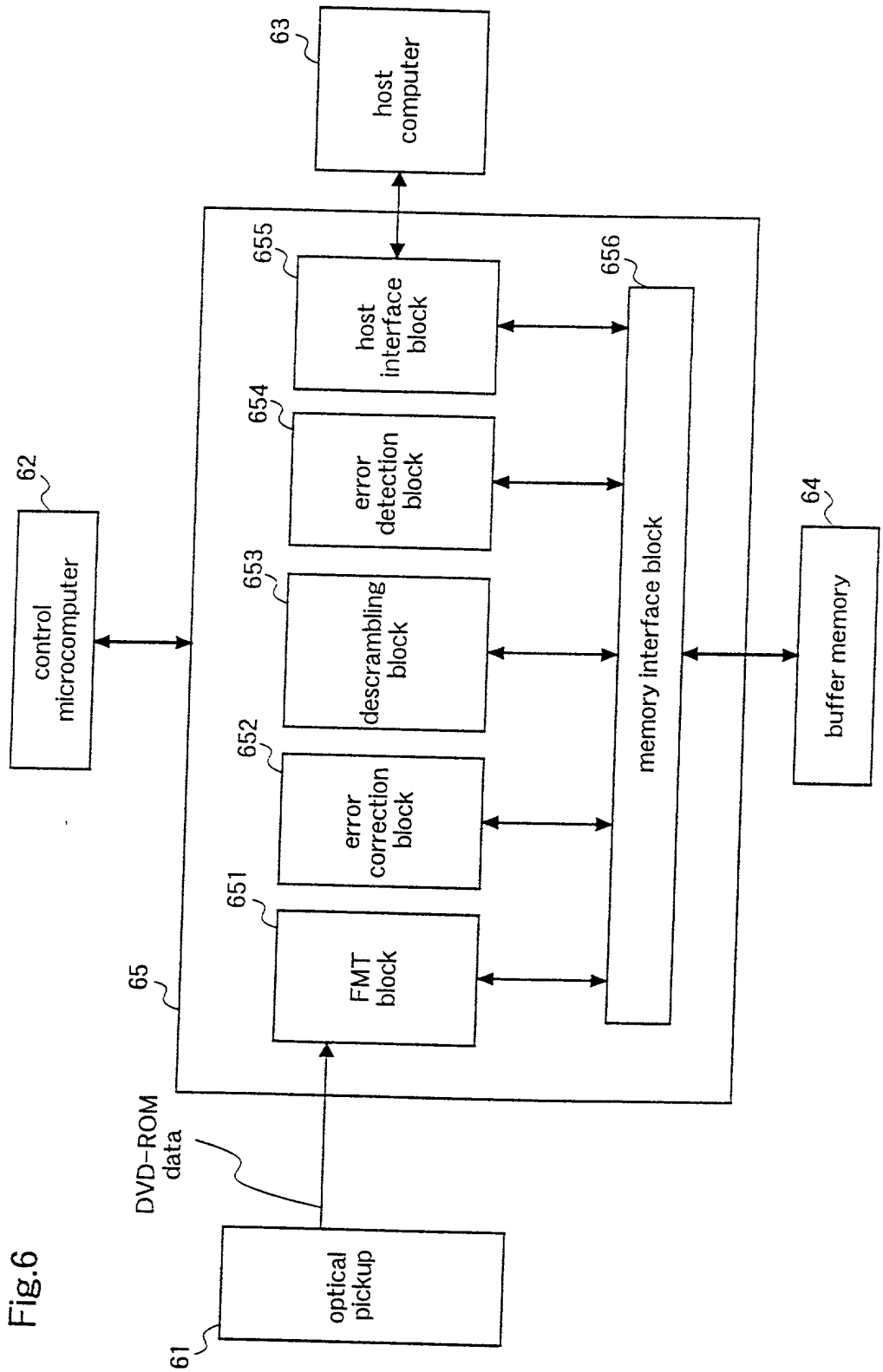

61
optical pickup
DVD-ROM data
65
62
control microcomputer
63
host computer
64
buffer memory
651
FMT block
652
error correction block
653
descrambling block
654
error detection block
655
host interface block
656
memory interface block

Fig.6

Rev. 3-21-01 Effective March 1998

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

() Original () Supplemental () Substitute (X) PCT () DESIGN

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title: SIGNAL PROCESSOR

of which is described and claimed in:
() the attached specification, or
() the specification in application Serial No. NEW, filed May 10, 2001, and with amendments through _____, or
(X) the specification in International Application No. PCT/JP00/06122, filed September 8, 2000, and as amended on May 10, 2001 (if applicable).

I hereby state that I have reviewed and understand the content of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code, §119 (and §172 if this application is for a Design) of any application(s) for patent or inventor's certificate listed below and have also identified below any application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
Japan	No.Hei.11-256736	September 10, 1999	YES

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

And I hereby appoint Michael R. Davis, Reg. No. 25,134; Matthew M. Jacob, Reg. No. 25,154; Warren M. Cheek, Jr., Reg. No. 33,367; Nils Pedersen, Reg. No. 33,145; Charles R. Watts, Reg. No. 33,142; and Michael S. Huppert, Reg. No. 40,268, who together constitute the firm of WENDEROTH, LIND & PONACK, L.L.P., as well as any other attorneys and agents associated with Customer No. 000513, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith.

I hereby authorize the U.S. attorneys and agents named herein to accept and follow instructions from HAYASE & CO. as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys and myself. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by me.

Direct Correspondence to Customer No:	Direct Telephone Calls to
000513 PATENT TRADEMARK OFFICE	WENDEROTH, LIND & PONACK, L L P 2033 "K" Street, N W , Suite 800 Washington, D C 20006-1021 Phone (202) 721-8200 Fax (202) 721-8250

Full Name of First Inventor	FAMILY NAME AOKI	FIRST GIVEN NAME Toru	SECOND GIVEN NAME	
Residence & Citizenship	CITY Ehime	STATE OR COUNTRY Japan	COUNTRY OF CITIZENSHIP Japan	
Post Office Address	ADDRESS Ko 2003-51, Shimoshimayama, Saijo-shi, Ehime 793-0006 Japan	CITY	STATE OR COUNTRY	ZIP CODE
Full Name of Second Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE
Full Name of Third Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE
Full Name of Fourth Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE
Full Name of Fifth Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE
Full Name of Sixth Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

I further declare that all statements made herein of my own knowledge are true, and that all statements on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1st Inventor Toru Aoki Date July 2, 2001
Toru AOKI

2nd Inventor ______ Date ______

3rd Inventor ______ Date ______

4th Inventor ______ Date ______

5th Inventor ______ Date ______

6th Inventor ______ Date ______

The above application may be more particularly identified as follows:

U.S. Application Serial No. NEW Filing Date May 10, 2001

Applicant Reference Number P-23070-02 Atty Docket No. 2001-0565A

Title of Invention SIGNAL PROCESSOR